UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/615,880	07/10/2003	Sabera Kazi	H0004522	8476

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EXAMINER
VLAHOS, SOPHIA

ART UNIT	PAPER NUMBER
2611	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	04/04/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

PTOL-90A (Rev. 10/06)

	Application No.	Applicant(s)
Office Action Summary	10/615,880	KAZI ET AL.
	Examiner	Art Unit	
	SOPHIA VLAHOS	2611	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE <u>3</u> MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.
- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 January 2007*.

2a)☒ This action is **FINAL.**   2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

    4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *16 January 2007* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

    Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

    a)☐ All   b)☐ Some * c)☐ None of:

      1.☐ Certified copies of the priority documents have been received.

      2.☐ Certified copies of the priority documents have been received in Application No. _____.

      3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

    * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1)☐ Notice of References Cited (PTO-892)

2)☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3)☐ Information Disclosure Statement(s) (PTO/SB/08)
    Paper No(s)/Mail Date _____.

4)☐ Interview Summary (PTO-413)
    Paper No(s)/Mail Date. _____ .

5)☐ Notice of Informal Patent Application

6)☐ Other: _____.

DETAILED ACTION

Response to Arguments

1.   Applicant's arguments filed 1/16/2007 have been fully considered but they are

not persuasive.

Page 10 of "Remarks" Applicatn argues: "Applicants assert that nothing in the

AAPA, Chung et al or Dutta, taken alone or together, teaches or suggests "a frequency

offset calculation circuit to determine a frequency offset between an oscillator in the

DPSK receiver and an oscillator in the DPSK transmitter by comparing the in-phase and

quadrature components with a second delayed, conjugated version of the in-phase and

quadrature components."

In addressing the above limitation in claim 1, the Examiner asserted that Chung

et al teaches "a frequency offset calculation circuit to determine a frequency offset by

comparing the in-phase and quadrature components with a second delayed, conjugated

version of the in-phase and quadrature components." OA p. 5. In support of this

assertion, the Examiner refers to paragraph 0005 of Chung. However, paragraph 5

merely discusses "a phase-increment extraction circuit 40" which "includes a delay

circuit 41, a conjugate circuit 42, and a multiplier 45." The phase-increment extraction

circuit 40 outputs "the phasor Rk" which "has an argument containing the phase

increment A0 rotated according to frequency offsets and the phase difference of

successive samples of the modulation." (emphasis added). Para. [0005]. In addition,

Chung discusses in paragraph 0005 "the argument circuit 30 extracts the phase Offset"

and "the frequency offset f can be estimated by using the phase offset of the phasor

Rk". "

Examiner disagrees with Applicant's assessment of the Chung reference and

points out that the carrier frequency offset manifests itself as phase rotation $\Delta\theta$ between

adjacent samples.

Page 11 of the "Remarks" Applicant argues: "...Hence, the phase-increment

extraction circuit in Chung does not teach or suggest a "frequency offset calculation

circuit frequency offset calculation circuit to determine a frequency offset between an

oscillator in the DPSK receiver and an oscillator in the DPSK transmitter by comparing

the in-phase and quadrature components with a second delayed, conjugated version of

the in-phase and quadrature components." At best, the phase-increment extraction

circuit of Chung et al. teaches a differential demodulator as discussed in the

background section of the present application. Since nothing in Chung et al., the AAPA,

or Dutta, taken alone or in combination, teaches or suggests all the claimed limitations

of claim 1, claim 1 is not obvious."

With respect to the claimed limitation: "...comparing the in-phase and quadrature

components with a second delayed, conjugated version of the in-phase and quadrature

components..." Paragraph [0005] and Fig. 1 of Chung et. al. show receiving symbol Zk

in-phase and quadrature components and comparing Zk to Zk-1 which is "...a second

delayed conjugated version of the in-phase and quadrature components;" therefore

Chung et. al., teaches the claimed limitation "...comparing the in-phase and quadrature

components with a second delayed, conjugated version of the in-phase and quadrature components..."

Therefore the 35 U.S.C. 103(a) rejections using the Chung et. al. reference are maintained

Page 16 of "Remarks" Applicant argues: In addressing the above limitation in claim 1, the Examiner asserted that LaBerge et al discloses "a frequency offset calculation circuit to determine a frequency offset between the DPSK receiver and the DPSK transmitter by comparing the in-phase and quadrature components with a second delayed, conjugated version of the in-phase and quadrature components." OA p. 9. In support of this assertion, the Examiner refers to the abstract, col. 5 lines 43-44, col. 4 lines 56-64, mad col. 6 lines 42-45. In addition, the Examiner refers to "the use of elements 15 (one bit delay), 16 (conjugate), 17 (coherent detector)" in Fig. 7. However, LaBerge el al. merely discusses "one of the advantages of the present invention is the removal of the effects of the unknown rotation wT. This is achieved by the application of the complex phase correction/rotation factor, r(t), after the DPSK demodulation process." col. 5 lines 43-47. With regards to phase correction/rotation factor r(t), LaBerge states "the complex output of lowpass filter 21 establishes a 'reference' estimate, r(t)." In addition, with regards to elements 15, 16, and 17 of Fig. 7, LaBerge states "this series of operations results in a sequence of complex values whose phase angles are a measure of the phase difference between two consecutive DPSK bits." Similarly, in an "exemplary conventional DPSK demodulator" discussed in the

background section of the present application "the current symbol is compared to the

prior symbol to determine relative phase difference between the current and previous

symbols." Para. [0007] (emphasis added).

Hence, the cited passages and elements 15, 16, and 17 in LaBerge et al. do not

teach or suggest a "frequency offset calculation circuit frequency offset calculation

circuit to determine a frequency offset between an oscillator in the DPSK receiver and

an oscillator in the DPSK transmitter by comparing the in-phase and quadrature

components with a second delayed, conjugated version of the in-phase and quadrature

components." At best, elements 15, 16, and 17 teach a differential demodulator as

discussed in the background section of the present application.

In response to the above arguments Examiner points out that LaBerge et. al.,

teaches that frequency drifts (including carrier frequency offset) result into phase

rotation (column 4, lines 60-64) and the coherent detector 17 is used to determine

phase difference between successive complex samples (see column 3, lines 2-5,

column 5,lines56-60))(shown in Fig. 7, comparison between complex (in-phase and

quadrature component) sample into 17 that is multiplied by delayed and conjugated

version of the complex sample).

Therefore the 35 U.S.C. 103(a) rejections using the LaBerge et. al. reference are

maintained.

Specification

2.   The amendments to the specification (see paragraphs [0011] and [0034])

received on 1/16/2007 are acceptable.

Drawings

3.   The drawings (Fig. 1, with "Prior Art" label added, Fig. 2-3 with corrections)were

received on 1/16/2007. These drawings are acceptable.

Claim Rejections - 35 USC § 103

4.   The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all

obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5.   Claims 1-3, 5, 7-9, 11-12, 14-16, 18-19, 21 are rejected under 35 U.S.C. 103(a)

as being unpatentable over the applicant's admitted prior art of the current application

(hereafter referred to as AAPA) in view of Dutta (U.S. 5,313,493) and Chung et. al.

(U.S. 2004/0190655).

        With respect to claim 1, the AAPA discloses:; a differential demodulator to

determine a demodulated phase by comparing the in-phase and quadrature

components with a first delayed, conjugated version of the in-phase and quadrature

components (see Fig. 2, section "differential demodulator" including elements 203, 204,

204 and signals processed there are understood to be complex (in-phase and

quadrature) since the conjugate operation of element 204 is meaningful for complex

signals, see paragraph [0007] of the specification) ; a frequency offset calculation circuit

to determine a frequency offset between an oscillator in the DPSK receiver and an

oscillator in the DPSK transmitter (Fig. 2, element 218, see paragraph [0011] of

specification); a frequency correction circuit to correct the demodulated phase using the

frequency offset into a corrected phase (Fig. 2, phase out of element 220, see last

sentence of paragraph [0011] of the specification); a phase correction circuit to

determine an absolute phase using the corrected phase (Fig. 2, elements 224, 226, see

paragraph [0012]); and a symbol mapping circuit to map the absolute phase to an

output symbol, comprising one or more bits of data (Fig. 2, element 226, see last

sentence of paragraph [0012]).

The AAPA does not expressly teach: means for converting the input signal to in-

phase and quadrature components, and a frequency offset calculation circuit to

determine a frequency offset between an oscillator in the DPSK receiver and an

oscillator in the DPSK transmitter by comparing the in-phase and quadrature

components with a second delayed, conjugated version of the in-phase and quadrature

components.

In the same field of endeavor, Dutta discloses: means for converting the input

signal to in-phase and quadrature components (see column 1, lines 46-51). At the time

of the invention, it would have been obvious to a person skilled in the art to use complex

baseband signal representation i.e. convert the input signal to in-phase and quadrature components in the receiver of the AAPA that includes the DPSK demodulator of Fig. 2, since DPSK information is contained in a vector including I and Q components (see Fig. 1 of the instant application).

In the same field of endeavor, Chung et. al., a frequency offset calculation circuit to determine a frequency offset by comparing the in-phase and quadrature components with a second delayed, conjugated version of the in-phase and quadrature components (see Fig. 1, output $\Delta\theta$ is the phase increment caused by frequency offsets (mentioned in middle of paragraph [0005] that describes the apparatus shown in Fig. 1) .

At the time of the invention, it would have been obvious to a person skilled in the art to use the frequency offset determining system of Chung et. al., in the system of the AAPA (substituting elements 218 and 220 since the system of Chung et. al, determines the phase offset caused by the frequency offset, therefore, element 220 is unnecessary) since (carrier) frequency offsets must be determined and corrected since they introduce phase rotation to the ideal signal phasor (i.e. distort the signal) (see paragraphs [0002]-[0004] of Chung et. al., where the (carrier) frequency offset is undesirable to the signal and has to be corrected).

With respect to claim 2, all of the limitations of claim 2 are analyzed above in claim 1, except for: comprising a glitch filter to filter the frequency offsets to remove noise and glitches caused by phase transients between symbols.

However, Chung et. al., discloses: removing noise and glitches caused by phase transients between symbols, see squaring operation of element 20 of Fig. 1, and second half of paragraph [0005] and all of paragraphs [0006]-[0007], where the squared phasor (that includes the frequency offset) that is insensitive to phase differences between successive modulated samples (understood to also include phase errors (transients) caused for example by non-ideal components), and see that the noise can be ignored). Therefore at the time of the invention, it would have been obvious to a person skilled in the art that the system (squaring, averaging operation) of Chung et. al., functions equivalently to a glitch filter that removes noise and glitches caused by phase transients between symbols.

With respect to claim 3, all of the limitations of claim 2 are analyzed above in claim 1, and the AAPA disclose: wherein the delay associated with the first delayed version of the I and Q components in the differential demodulator is approximately one symbol interval (see Fig. 2, delay Z has Tsym duration and see last sentence of paragraph [0007] of specification).

With respect to claim 5, all of the limitations of claim 1 are analyzed above in claim 1 and the AAPA discloses: further comprising an optimal sample calculation circuit to determine an optimal sample to use to determine the demodulated phase and the frequency offset (see Fig. 2, elements 210, 212, 214, and the control of switches 208 and 216 see paragraphs [0008]-[0009] of the specification).

With respect to claim 7, all of the limitations of claim 7 are analyzed above in claim 5, and claim 7 is analyzed similarly to claim 2 above.

With respect to claim 8, claim 8 is analyzed similarly to claim 1 above, and with respect to the limitations: receiving the DPSK signal; digitizing the DPSK signal, in the same field of endeavor, Dutta et. al., discloses: receiving the PDPSK signal; digitizing the PDPSK signal (see Fig. 4, the PDPSK communication system, receiver and transmitter, the receiver includes antenna to received the transmitted PDPSK signals and see column 7, lines 35-38 where digital signal implies converting to digital signals at the receiver side of Fig. 4). At the time of the invention, it would have been obvious to a person skilled in the art that receiving the DPSK signal (with an antenna as shown by Dutta for the PDPSK signal) and digitizing the DPSK signal (as implied by Dutta) since receiving and digitizing signals is very well in the art and is an integral part of communication receivers and allows for use of DSPs (allow for fast processing, miniaturization since they can be combined with other digital components).

With respect to claims 9, 11, 12, 14 these claims are analyzed similarly to claims 3, 2, 5, and 7 above.

Claims 15, 16, 18-19, 21 are analyzed similarly to claims 1, 3, 2, 5, and 7 above.

6.   Claims 1, 3-5, 8- 10,12 15, 17 are rejected under 35 U.S.C. 103(a) being

unpatentable over the applicant's admitted prior art of the current application (hereafter

referred to as AAPA) in view of LaBerge et. al. (U.S. 5,142,287).

        With respect to claim 1, the AAPA discloses:; a differential demodulator to

determine a demodulated phase by comparing the in-phase and quadrature

components with a first delayed, conjugated version of the in-phase and quadrature

components (see Fig. 2, section "differential demodulator" including elements 203, 204,

204 and signals processed there are understood to be complex (in-phase and

quadrature) since the conjugate operation of element 204 is meaningful for complex

signals, see paragraph [0007] of the specification) ; a frequency offset calculation circuit

to determine a frequency offset between an oscillator in the DPSK receiver and an

oscillator in the DPSK transmitter (Fig. 2, element 218, see paragraph [0011] of

specification); a frequency correction circuit to correct the demodulated phase using the

frequency offset into a corrected phase (Fig. 2, phase out of element 220, see last

sentence of paragraph [0011] of the specification); a phase correction circuit to

determine an absolute phase using the corrected phase (Fig. 2, elements 224, 226, see

paragraph [0012]); and a symbol mapping circuit to map the absolute phase to an

output symbol, comprising one or more bits of data (Fig. 2, element 226, see last

sentence of paragraph [0012]).

        The AAPA does not expressly teach: means for converting the input signal to in-

phase and quadrature components, and a frequency offset calculation circuit to

determine a frequency offset between an oscillator in the DPSK receiver and an

oscillator in the DPSK transmitter by comparing the in-phase and quadrature

components with a second delayed, conjugated version of the in-phase and quadrature

components.

In the same field of endeavor, LaBerge et. al. disclose: means for converting the

input signal to in-phase and quadrature components (see column 2, lines 54-56), and a

frequency offset calculation circuit to determine a frequency offset between the DPSK

receiver and the DPSK transmitter by comparing the in-phase and quadrature

components with a second delayed, conjugated version of the in-phase and quadrature

components (see abstract, column 5, lines 43-44, and column 4, lines 56-64,

interpreted as referring to phase rotation cause caused by unknown frequency drift,

(see for example Doppler shifts mentioned in column 4, lines 60-66) and also see

column 6, lines 42-45, where phase wT or wT + π cane be determined).

At the time of the invention, it would have been obvious to a person skilled in the

art to use the apparatus and teachings of LaBerge et. al., (for example as shown in Fig.

7, the use of elements 15 (one bit delay), 16 (conjugate), 17 (coherent detector) that

process complex signals, and generate Vc(t), see column 6, lines 42-45 out of which the

phase offset corresponding to the frequency error), to determine a frequency offset

between an oscillator in the DPSK receiver and an oscillator in the DPSK transmitter by

comparing the in-phase and quadrature components with a second delayed, conjugated

version of the in-phase and quadrature components, (similarly to the Doppler shift

caused frequency error, non-ideal components such as oscillators also contribute to

frequency errors) since it is known in the art that frequency errors/shifts result into

phase shifts that distort the received signals and have to be taken into account and

compensated for at the receiver (also see abstract of LeBerge et. al.).

With respect to claim 3, all of the limitations of claim 2 are analyzed above in

claim 1, and the AAPA disclose: wherein the delay associated with the first delayed

version of the I and Q components in the differential demodulator is approximately one

symbol interval (see Fig. 2, delay Z has Tsym duration and see last sentence of

paragraph [0007] of specification).

With respect to claim 4, all of the limitations of claim 4 are analyzed above in

claim 1, and LaBerge et. al., discloses: wherein the delay associated with the I and Q

components in the frequency offset calculation circuit is approximately one sample

interval (see abstract, (especially the …removal of effects of unknown frequency

component…) and column 4, lines 7-13, 45-60, where the sample interval is interpreted

to correspond to the bit time and also see column 5, lines 66-67, and column 6, lines 1-

18, 42-45, where the phase corresponding to the wT is the unknown frequency rotation

(column 5, lines 43-44)).

With respect to claim 5, all of the limitations of claim 1 are analyzed above in

claim 1 and the AAPA discloses: further comprising an optimal sample calculation circuit

to determine an optimal sample to use to determine the demodulated phase and the

frequency offset (see Fig. 2, elements 210, 212, 214, and the control of switches 208 and 216 see paragraphs [0008]-[0009] of the specification).

With respect to claim 8, claim 8 is analyzed similarly to claim 1, above and with respect to the additional limitations: receiving the DPSK signal; digitizing the DPSK signal;, LaBerge et. al., disclose the above in column 3, lines 43-45, 52-67, (reception of IF signal that uses DPSK, and A/D conversion of the received signal)

With respect to claims 9-10, 12, these claims are analyzed similarly to claims 3-5 above.

With respect to claims 15, 17 these claims are analyzed similarly to claims 1,3-5 respectively.

7.   Claims 6, 13, 20 are rejected under 35 U.S.C. 103(a) being unpatentable over the applicant's admitted prior art of the current application (hereafter referred to as AAPA) in view of LaBerge et. al. (U.S. 5,142,287) as applied to claims 5, 12, 19 respectively, and in view of Legrand et. al., (U.S. 6,74,822).

With respect to claim 6, all of the limitations of claim 6, are analyzed above in claim 5, except for: wherein the optimal sample calculation circuit determines the optimal sample as the sample associated with a peak amplitude of the combined in-phase and quadrature components of each sample in each symbol interval.

In the same field of endeavor, Legrand et. al., disclose: wherein the optimal sample calculation circuit determines the optimal sample as the sample associated with a peak amplitude each sample in each symbol interval (see column 1, lines 62-67, column 2, lines 7, column 3, lines 40-42, where the sample (and subsequently the sampling instant) with the maximum value is determined and keeps updating). At the time of the invention, it would have been obvious to a person skilled in the art at the time of the invention, to use the teachings of Legrand in the system of the AAPA, to determine the optimal sample as the sample associated with a peak amplitude (maximum value) of the combined in-phase and quadrature components of each sample in each symbol interval (the combined in-phase and quadrature components would be used since the system of AAPA processes complex signals and finding the peak value of the samples would involve using the in-phase and quadrature components). The benefit of using the teachings of Legrand et. al., in the system of the AAPA (to perform best sample selection) include: limiting the number of computations and operating costs (see column 1, lines 49-51 of Legrand et. al.,)

With respect to claims 13, and 20 these claims are analyzed similarly to claim 6 above.

Conclusion

8.   The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Hunag et. al., (U.S. 5,991,289) disclose: a method and system for symbol, frame , and carrier synchronization for OFDM signals.

Mui (U.S. 5,432,819) discloses: a phase and frequency trackers used in a DPSK receiver.

Dutta (U.S. 5,450,447) discloses: AFC loop used in a PSK based system.

Kim (U.S. 7,058,151) discloses: frequency and timing synchronization for OFDM signals.

Tsuda et. al., (U.S. 5,440,267): a pi/4 shift QPSK receiver using a frequency error offset estimating circuit that corrects for transmitter/receiver frequency offsets.
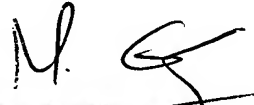

Contact Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to SOPHIA VLAHOS whose telephone number is 571 272 5507. The examiner can normally be reached on MTWRF 8:30-17:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mohammed Ghayour can be reached on 571 272 3021. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

SV
3/22/07

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